ABSTRACT OF THE DISCLOSURE

A MOS transistor having a recessed gate electrode and a fabrication method thereof are provided. The MOS transistor includes an isolation layer formed at a predetermined region of a semiconductor substrate to define an active region and double trench regions formed in the active region. The double trench region is composed of an upper trench region crossing the active region and a lower trench region located under the upper trench region. Thus, the active region is divided into two sub-active regions. Sidewalls of the upper trench region are covered with a spacer, which is used as an etching mask to form the lower trench region in the semiconductor substrate of the upper trench region. The upper and lower trench regions are then filled with a gate electrode. Also, high concentration source/drain regions are formed at the top surfaces of the sub-active regions respectively. Therefore, an effective channel length of the MOS transistor is determined according to the dimension of the lower trench region.